leaked to the outside loop such that the outside loop might be constructed with a relatively narrow bandwidth in order to provide for more accurate tracking capability once the carrier has been acquired.

In the Claims:

Page 61, line 3, replace the word CLAIMS with: WHAT IS CLAIMED

Please amend claims 12, 88, 96, and 101 as follows:

1. A method for operating a receiver having a particular sampling frequency related to a symbol rate to recover carrier and timing information from a received spectrum including a pilot signal, comprising:

centering the received spectrum at a known position relative to baseband;

tracking the pilot signal with a phase-lock-loop;

evaluating the frequency of the pilot signal with respect to the sampling frequency; and

adjusting the centering of the received spectrum until the evaluated frequency of the pilot is in integral relationship with the sampling frequency.

2. The method according to claim 1, further comprising:

filtering the received spectrum in a low pass filter having a cut-off frequency related to the sampling frequency;

processing the filtered signal in a high pass filter having a cut-off frequency related to the sampling frequency; and

wherein the low pass and high pass filters define an equivalent bandpass filter, the equivalent bandpass filter defining upper and lower sideband regions each centered at an expected position of the pilot signal.

3. The method according to claim 2, wherein the received spectrum exhibits a raised cosine response characteristic, the upper and lower sideband regions of the equivalent filter including transition regions of the spectra defined by the high pass and low pass filters.

4. The method according to claim 3, wherein the receiver's sampling frequency is determined such that the pilot frequency is equal to about one fourth the sampling frequency.

5. The method according to claim 4, wherein the high pass filter is a Nyquist prefilter having a lower cut-off frequency at about one fourth the sampling frequency, the high pass filter centering the spectrum at a frequency about one half the sampling frequency.

6. The method according to claim 5, wherein the low pass filter is a square root Nyquist filter having an upper cutoff frequency at about one fourth the sampling frequency, the square root Nyquist filter centering the spectrum at about baseband.

7. The method according to claim 6, the desired position of the pilot signal being substantially centered in each transition region, thereby causing the desired position of the pilot signal to be centered in each of the upper and lower sideband regions of the equivalent filter at a frequency substantially equal to one fourth the sampling frequency, thereby augmenting a signal occurring at one fourth the sampling frequency.

8. The method according to claim 7, further comprising:

receiving a sideband region from the equivalent filter in a tracking loop;

sweeping the sideband region to identify an augmented frequency component;

comparing the augmented frequency component to the expected frequency of the pilot signal; and

shifting the sampling frequency in a direction and an amount such that the augmented frequency component coincides with the expected frequency of the pilot signal.

9. The method according to claim 8, further comprising the step of using the shifted sampling frequency to define a symbol timing reference signal.

10. A digital communication system, comprising:

a front end receiving an input spectrum at an intermediate frequency, the input spectrum including an inserted predetermined frequency component;

first and second nested tracking loops, the first loop acquiring carrier frequency lock in operative response to the predetermined frequency component of the received spectrum, the second loop providing a signal adapted to position the spectrum at a predetermined location relative to baseband in operative response to said predetermined frequency component; and

a third tracking loop coupled to define a symbol timing parameter in operative response to said same predetermined frequency component.

11. The digital communication system according to claim 10, further comprising an equivalent filter operating on the received spectrum in order to define a pair of symmetric signals, each of the symmetric signals centered at the characteristic frequency of the predetermined frequency component when the received spectrum is at baseband.

12. (Amended) The digital communication system according to claim 11, wherein symbol timing is performed at a sampling frequency, the system further comprising:

a first filter having a high-pass characteristic and a lower cut-off frequency related to the sampling frequency;

a second filter having a low pass characteristic and an upper cut-off frequency related to the sampling frequency; and

wherein the first and second filters define an equivalent bandpass filter having symmetric passband regions centered about a frequency related to the sampling frequency.

13. The digital communication system according to claim 12, wherein the received spectrum exhibits a raised cosine response characteristic, the passband regions including the transition regions of the high and low pass filtered spectra.

14. The digital communication system according to claim 13, wherein the sampling frequency is chosen such that the predetermined frequency component is disposed at a frequency one fourth the sampling frequency.

15. The digital communication system according to claim 14, wherein the high pass filter has a lower cut-off of about one fourth the sampling frequency and a passband center of about one half the sampling frequency.

16. The digital communication system according to claim 15, wherein the low pass filter has an upper cut-off of about one fourth the sampling frequency, the equivalent filter passbands thereby centered at a frequency about one fourth the sampling frequency.

17. The digital communication system according to claim 16, wherein the inserted predetermined frequency component is a pilot signal disposed at a location along the spectrum normally reserved for a suppressed carrier when the spectrum is a conventional terrestrial broadcast spectrum, the pilot signal centered in the equivalent filter's passband regions when the sampling frequency is one fourth the frequency of the pilot signal.

18. The digital communication system according to claim 17, further comprising:

a phase/frequency detector coupled to receive an equivalent filter passband signal;

means for determining whether the pilot is centered in the passband region; and

an oscillator circuit developing a timing reference signal having a frequency related to the sampling frequency, the oscillator circuit increasing or decreasing the timing reference signal frequency in operative response to the position of the pilot signal with respect to a passband region center.

19. An integrated circuit receiver including a decision directed carrier phase recovery circuit for complex signals representing symbols characterized by in-phase and quadrature-phase portions separated in time by an offset, the carrier phase recovery circuit comprising:

a sampling circuit configured to sample each of the in-phase and quadrature-phase portions of the complex signal at an in-phase sampling time and at a quadrature-phase sampling time separated by an offset;

a separation circuit, connected to separate the sampled, in-phase, signal into an in-phase sample time data stream and an in-phase time offset data stream;

a decision circuit, connected to receive the in-phase sample time data stream and generate a tentative symbolic decisions from in-phase sampled data;

a summing circuit coupled to combine the tentative symbolic decisions with signals from the in-phase sample time data stream to generate an in-phase symbolic error term;

a multiplier circuit connected to combine the in-phase symbolic error term with a time offset signal representing the quadrature-phase portion of the complex signal.

20. The carrier phase recovery circuit according to claim 19, further comprising:

a phase error term representing the in-phase portion, generated by the multiplier;

a loop filter;

a reference synthesizer circuit; and

a phase correction circuit, the reference synthesizer providing phase correction signals to the phase correction circuit in operative response to the phase error term.

21. The carrier phase recovery circuit according to claim 19, further comprising:

a second separation circuit, connected to separate the sampled, quadrature-phase, signal into a quadrature-phase sample time data stream and a quadrature-phase time offset data stream;

a second decision circuit, connected to receive the quadrature-phase sample time data stream and generate a tentative symbolic decisions from quadrature-phase sampled data;

a second summing circuit coupled to combine the tentative symbolic decisions with signals from the quadrature-phase sample time data stream to generate a quadrature-phase symbolic error term;

a second multiplier circuit connected to combine the quadrature-phase symbolic error term with the a time offset signal representing the in-phase portion of the complex signal.

22. The carrier phase recovery circuit according to claim 21, wherein the second multiplier circuit combines the quadrature-phase symbolic error term with the in-phase time offset signal to develop a quadrature-phase phase error term.

23. The carrier phase recovery circuit according to claim 22, further comprising a multiplexer connected to each multiplier circuit, the multiplexer providing a signal stream of alternating in-phase and quadrqature-phase phase error terms to the loop filter.

24. The carrier phase recovery circuit according to claim 20, wherein the time offset signal representing the quadrature-phase portion of the complex signal is the sign of a quadrature-phase time offset data stream.

25 The carrier phase recovery circuit according to claim 20, wherein the time offset signal representing the quadrature-phase portion of the complex signal is a quadrature-phase time offset data stream.

26. The carrier phase recovery circuit according to claim 20, wherein the time offset signal representing the quadrature-phase portion of the complex signal is the Hilbert transform of the in-phase sample time data stream.

27. The carrier phase recovery circuit according to claim 20, further comprising:

a Hilbert transform circuit connected to receive the in-phase sample time data stream and output its Hilbert transform, wherein the time offset signal representing the quadrature-phase portion of the complex signal is the Hilbert transform of the in-phase sample time data stream; and

wherein the multiplier combines the symbolic in-phase error term with the Hilbert transform of the in-phase sample time data stream.

28. The carrier phase recovery circuit according to claim 27, further comprising:

a DFE coupled, in parallel fashion, with the decision device, the DFE providing correction signals for removing an ISI component from tentative symbolic decisions; and

a combining circuit coupled to combine DFE correction signals with in-phase sample time data.

29. The carrier phase recovery circuit according to claim 27, further comprising a delay matching circuit disposed between the summing circuit and the multiplier, the delay matching circuit providing a delay to the symbolic in-phase error term equal to a delay imposed by the Hilbert transform circuit.

30. In an integrated circuit receiver for coherently demodulating complex signals representing symbols, characterized by first-phase and second-phase portions, separated in time by an offset, a method for decision directed carrier phase recovery comprising:

sampling each of the first-phase and second-phase portions of the complex signal at a first-phase sampling time and at a second-phase sampling time separated from the first-phase sampling time by an offset;

separating the sampled first-phase signal into a sample-time data stream and a time-offset data stream;

making a tentative symbolic decision on signals from the first-phase sample-time data stream;

combining the tentative decisions with signals from the first-phase sample-time data stream to generate a symbolic first-phase error term;

multiplying the symbolic first-phase error term with a signal representing the time-offset sampled signal of the second-phase portion of the complex signal.

31. The method according to claim 30, further comprising:

separating the sampled second-phase signal into a sample-time data stream and a time-offset data stream;

making a tentative symbolic decision on signals from the second-phase sample-time data stream;

combining the tentative decisions with signals from the second-phase sample-time data stream to generate a symbolic second-phase error term;

multiplying the symbolic second-phase error term with a signal representing the time-offset sampled signal of the first-phase portion of the complex signal.

32. The method according to claim 30, further comprising:

defining a phase error term, representing the result of the multiplication of the symbolic first-phase error term with the time-offset sampled signal representing the second-phase portion of the complex signal; and

controlling a reference synthesizer to provide phase correction signals to a phase correction circuit in operative response to the phase error term.

33. The method according to claim 32, wherein the first-phase and second-phase portions of the complex signal are its in-phase and quadrature-phase components.

34. The method according to claim 33, wherein an in-phase sample-time signal corresponds to a quadrature-phase time-offset signal and a quadrature-phase sample-time signal corresponds to an in-phase time-offset signal.

35. The method according to claim 30, wherein the signal representing the time-offset sampled signal of second-phase portion of the complex signal is the sign of the time-offset sampled signal.

36. The method according to claim 30, wherein the step of separating the sampled first-phase signal into a sample-time data stream and a time-offset data stream comprises taking the Hilbert transform of the first-phase sample-time data stream.

37. An integrated circuit comprising:

a decision directed symbol error magnitude determination circuit;

a symbol rotation direction indication circuit; and

wherein the symbol error magnitude circuit operative in response to a first-phase portion of a complex signal, the symbol rotation direction indication circuit operative in response to a second -phase portion of the complex signal, the first-phase and second-phase portions offset from one another.

38. An integrated circuit comprising:

a decision directed symbol error magnitude determination circuit;

a symbol rotation direction indication circuit; and

wherein the symbol error magnitude circuit operative in response to a first-phase portion of a complex signal, the symbol rotation direction indication circuit operative in response to a Hilbert transform of the first-phase portion.

39. The integrated circuit according to claim 37, the decision directed symbol error magnitude circuit further comprising:

a first-phase signal;

a decision circuit outputting first-phase decisions; and

an error circuit summing an first-phase decision with a first-phase signal to define a first-phase error term.

40. The integrated circuit according to claim 39, the symbol rotation direction indication circuit further comprising:

a signal representing a second-phase midpoint signal; and

a combining circuit, combining the first-phase error term with the signal representing the second-phase midpoint signal.

41. The integrated circuit according to claim 40, wherein the first-phase signal is an in-phase component of an offset complex signal.

42. The integrated circuit according to claim 41, wherein the second-phase midpoint signal is a quadrature-phase component of an offset complex signal.

43. The integrated circuit according to claim 42, wherein the signal representing the quadrature-phase midpoint signal is the sign of the quadrature-phase midpoint signal.

44. The integrated circuit according to claim 43, wherein the quadrature-phase midpoint signal corresponds to an offset quadrature-phase signal sampled at an in-phase sample time.

45. A method of operating an integrated circuit, comprising:
providing a decision directed symbol error magnitude circuit;
providing a symbol rotation direction indication circuit; and
wherein the symbol error magnitude circuit operative in response to a first-phase portion of a complex signal, the symbol rotation direction indication circuit operative in response to a second -phase portion of the complex signal, the first-phase and second-phase portions offset from one another.

46. A method of operating an integrated circuit, comprising:
providing a decision directed symbol error magnitude circuit;
providing a symbol rotation direction indication circuit; and
wherein the symbol error magnitude circuit operative in response to a first-phase portion of a complex signal, the symbol rotation direction indication circuit operative in response to a Hilbert transform of the first-phase portion.

47. The method according to claim 45, further comprising:
providing a first-phase signal;
providing first-phase decisions from a decision circuit; and
summing a first-phase decision with a first-phase signal to define a first-phase error term.

48. The method according to claim 47, further comprising:

providing a signal representing a second-phase midpoint signal; and

combining the first-phase error term with the signal representing the second-phase midpoint signal to define a phase error term.

49. An integrated circuit receiver comprising:

at least one timing loop;

a decision feedback equalizer including;

a feedforward filter; and

a decision feedback filter; and

a maximum likelihood sequence estimation circuit, coupled to receive input symbol samples from the feedforward filter, the maximum likelihood sequence estimation circuit integrated into the timing loop so as to provide enhanced reliability symbolic decisions to an input of the timing loop.

50. The integrated circuit receiver according to claim 49, the receiver operating on a complex signal transmitted in accordance with an 8-VSB modulation scheme, the receiver further comprising:

a summing circuit coupled in parallel fashion across the maximum likelihood sequence estimation circuit, the summing circuit combining input signal samples with symbolic decision output from the sequence estimation circuit to define a sequence estimated error term.

51. The integrated circuit receiver according to claim 50, wherein the feedforward filter includes adaptively updateable coefficient taps, the sequence estimated error term being provided to the feedforward filter to drive the tap updates.

52. The integrated circuit receiver according to claim 50, wherein the decision feedback filter includes adaptively updateable coefficient taps, the sequence estimated error term being provided to the decision feedback filter to drive the tap updates.

53. The integrated circuit receiver according to claim 50, wherein the maximum likelihood sequence estimation circuit is a trellis decoder, the trellis decoder including:

a decision device, receiving input symbol samples from the feedforward filter;

a path metric circuit for tracking a symbol sample's time history and for determining a symbolic decision likelihood based on a symbol sample's historical sequence; and

a path traceback circuit for storing a plurality of sequential symbolic decisions, the output of the traceback circuit outputting at least a final decision corresponding to a maximum symbolic decision likelihood based on a symbol sample's historical sequence.

54. The integrated circuit receiver according to claim 53, the traceback circuit coupled to output each of a plurality of intermediate symbolic decisions, each corresponding to a particular symbolic decision along the sequence.

55. The integrated circuit receiver according to claim 54, the traceback circuit having a length N, wherein N corresponds to the number of symbolic decision estimations within a sequence, each estimation represented by a circuit delay 1/N, each of the plurality of intermediate symbolic decisions separated from one another in time by an integer relationship with 1/N.

56. The integrated circuit receiver according to claim 55, wherein selected ones of the plurality of intermediate symbolic decisions are chosen for outputting based on a characteristic total delay of each selected one.

57. The integrated circuit receiver according to claim 56, further comprising:

a carrier recovery loop operating to detect a difference in phase or frequency between a signal input to the trellis decoder and a symbolic decision output from the trellis decoder;

wherein the decision feedback filter provides a compensation signal based on a symbolic decision output from the trellis decoder; and

wherein the carrier recovery circuit operates on an intermediate symbolic decision occurring earlier in the sequence than the symbolic decision provided the decision feedback filter.

58. The integrated circuit receiver according to claim 56, further comprising a timing recovery loop operating to detect a difference in phase or frequency between a signal input to the trellis decoder and a symbolic decision output from the trellis decoder wherein the carrier recovery circuit operates on an intermediate symbolic decision occurring earlier in the sequence than symbolic decision provided the timing recovery loop.

59. In an integrated circuit receiver, a method for operating a decision feedback equalizer, the method comprising:

providing a maximum likelihood sequence estimation circuit, including a symbolic traceback memory, the maximum likelihood sequence estimation circuit coupled to receive input symbol samples from a feedforward filter;

inputting a symbolic decision, representing a best survivor path of the symbolic traceback memory, to the decision feedback equalizer;

generating a sequence estimated symbolic error term from the best survivor path symbolic decision; and

providing the sequence estimated symbolic error term to the decision feedback equalizer as a tap coefficient update signal.

60. The method according to claim 59, wherein the maximum likelihood sequence estimation circuit includes:

a decision device, receiving input symbol samples from the feedforward filter;

a path metric circuit for tracking a symbol sample's time history and for determining a symbolic decision likelihood based on a symbol sample's historical sequence; and

wherein the symbolic traceback memory stores a plurality of sequential symbolic decisions, the output of the traceback memory outputting at least a final decision corresponding to a maximum symbolic decision likelihood based on a symbol sample's historical sequence.

61. The method according to claim 60, further comprising:

providing a symbolic decision, representing a best survivor path of the symbolic traceback memory to an input of a timing recovery circuit;

detecting a difference in phase or frequency between the symbolic decision and an input symbol sample; and

operating a de-rotator circuit in accordance with the comparison result.

62. The method according to claim 61, wherein the symbolic traceback memory stores a plurality of sequential symbolic decisions, the output of the traceback memory outputting at least a final decision corresponding to a maximum symbolic decision likelihood based on a symbol sample's historical sequence.

63. The method according to claim 62, wherein the symbolic traceback memory is further coupled to output a plurality of intermediate symbolic decisions, each corresponding to a particular symbolic decision along the sequence.

64. The method according to claim 63, the traceback circuit having a length N, wherein N corresponds to the number of symbolic decision estimations within a sequence, each estimation represented by a circuit delay 1/N, each of the plurality of intermediate symbolic decisions separated from one another in time by an integer relationship with 1/N.

65. The method according to claim 64, wherein selected ones of the plurality of intermediate symbolic decisions are chosen for outputting based on a characteristic total delay of each selected one.

66. The method according to claim 65, wherein the timing recovery circuit operates on an intermediate symbolic decision occurring earlier in the sequence than the symbolic decision provided the decision feedback filter.

67. An integrated circuit receiver, including an adaptive decision feedback equalizer, comprising:

a feedforward filter;

a decision circuit;

a decision feedback filter coupled in parallel fashion with the decision circuit; and

an offset generation circuit, wherein the offset generation circuit provides an offset signal to an output signal from the decision feedback filter, the offset signal corresponding to a bitwise representation of a DC component.

68. The integrated circuit receiver according to claim 67, further comprising:

a complex input signal corresponding to a multi-level constellation of symbols, each symbol represented by a number of bits; and

wherein the number of bits representing each symbol is determined by a power of two which identifies a size of the constellation.

69. The integrated circuit receiver according to claim 68, wherein the bit representation of the constellation includes a fixed offset term.

70. The integrated circuit receiver according to claim 69, wherein the fixed offset term is capable of representation by adding an additional bit to each number bits representing a symbol.

71. The integrated circuit receiver according to claim 70, wherein the offset signal corresponds to a digital value determined by the additional bit.

72. The integrated circuit receiver according to claim 71, wherein the constellation is a 256-QAM constellation and the number of bits representing each symbol is four, the offset signal corresponding to a -1/2 bit offset in the representation of QAM signals.

73. An integrated circuit receiver operating on a constellation of complex symbols, each symbol represented by a number N of bits, the receiver comprising:

an adaptive decision feedback equalizer including:

a decision feedback filter, constructed to receive a symbol decision having a wordlength of N-1 bits, the decision feedback filter outputting a compensated symbol decision having a wordlength of N-1 bits;

an offset generation circuit, generating a DC value corresponding to an Nth bit representation; and

a summing circuit for combining the decision feedback filter output and the DC value generated by the offset generation circuit.

74. The integrated circuit receiver according to claim 73, wherein the offset generation circuit is a filter.

75. The integrated circuit receiver according to claim 74, further comprising:

a feedforward filter; and

a decision circuit, coupled in parallel fashion with the decision feedback filter, the decision circuit outputting an N-1 bit wide word representing symbol decisions and a symbol error term.

76. The integrated circuit receiver according to claim 75, wherein the symbol error term adaptively trains filter coefficients of the decision feedback filter, the decision feedback filter coefficients provided to the offset generation circuit.

77. An integrated circuit receiver operating on a constellation of complex symbols, each symbol capable of representation by a digital word having a wordlength N of bits, the receiver comprising:

a feedback filter, constructed to receive an input stimulus signal having a wordlength of N-1 bits the feedback filter outputting a a signal having a wordlength of N-1 bits;

a correction filter constructed to provide an output signal having a single bit representation; and

means for combining the feedback filter output and the correction filter output to define a signal having a value consistent with an N-bit representation.

78. The integrated circuit receiver according to claim 77, wherein the correction filter outputs a signal corresponding to a fixed offset term introduced by a representation of complex symbols in a first numbering system.

79. The integrated circuit receiver according to claim 77, wherein the correction filter outputs a signal corresponding to a fixed offset term introduced by a pilot tone inserted into a transmitted spectrum.

80. The integrated circuit receiver according to claim 77, wherein the correction filter outputs a signal corresponding to a fixed offset term representing the sum of a fixed offset introduced by a representation of complex symbols in a first numbering system and a fixed offset introduced by a pilot tone inserted into a transmitted spectrum.

81. The integrated circuit receiver according to claim 77, further comprising:

a feedforward filter; and

a decision device, coupled in parallel fashion with the feedback filter, the decision device outputting symbolic decisions in an N-1 bit representation and further outputting a symbolic error term associated with each decision.

82. The integrated circuit receiver according to claim 81, wherein the symbolic error term adaptively trains filter coefficients of the feedback filter, the feedback filter providing an ISI compensation to symbolic decisions expressed in an N-1 bit representation.

83. The integrated circuit receiver according to claim 82, wherein the correction filter receives filter coefficients from the feedback filter, the correction filter providing an ISI compensation to a fixed offset term.

84. The integrated circuit receiver according to claim 83, the constellation comprising a 256-QAM constellation, each real and each imaginary symbol represented by a 5-bit word in two's

compliment notation, the 5-bit word comprising a 4-bit portion expressing each symbol's relative position within the constellation and a 1-bit portion expressing a fixed offset between each symbol's relative position and its absolute position within the constellation.

85. In an integrated circuit receiver, a method for adaptively equalizing symbols expressed as a digital word, the method comprising:

identifying a nibble component of the word, the nibble component representing a fixed offset value;

truncating the word to a vestigal representation excluding the nibble component;

convolving the vestigal representation with coefficient taps in a first filter;

convolving the fixed offset value, corresponding to the excluded nibble component, with coefficient taps in a second filter; and

summing the convolutions.

86. The method according to claim 85, wherein the first filter is a decision feedback filter.

87. The method according to claim 86, wherein the second filter is a DC correction filter.

88. (Amended) A digital communication system for receiving signals modulated in accordance with a multiplicity of modulation formats, comprising:

a front end receiving an input spectrum at an intermediate frequency;

first and second nested carrier tracking loops, the first loop acquiring carrier frequency lock in operative response to a predetermined frequency component inserted into the received spectrum, the second loop providing a signal adapted to position the spectrum at a predetermined location relative to baseband in operative response to said predetermined frequency component;

a third tracking loop coupled to define a symbol timing parameter in operative response to said same predetermined frequency component;

an equivalent filter operating on the received spectrum in order to define a pair of symmetric signals, each of the symmetric signals centered at the characteristic frequency of the predetermined frequency component when the received spectrum is at baseband;

a decision directed carrier phase recovery loop having a phase detector operative with respect to each of the multiplicity of modulation formats;

an adaptive decision feedback equalizer, including;

a feedforward filter;

a decision feedback filter;

a single bit LMS derotator coupled to adjust phase offset of signals directed to the adaptive decision feedback equalizer; and

a maximum likelihood sequence estimation circuit, coupled to receive input symbol samples from the feedforward filter, the maximum likelihood sequence estimation circuit integrated into a timing loop so as to provide enhanced reliability symbolic decisions to an input of the timing loop.

89. The digital communication system according to claim 88, wherein the multiplicity of modulation formats includes vestigal sideband modulation (VSB), quadrature amplitude modulation (QAM) and offset-quadrature amplitude modulation (OQAM).

90. The digital communication system according to claim 89, further comprising:

a first derotator coupled into the signal path in a position after the front end, the derotator converting the received spectrum to a position relative to baseband signal in response to the first tracking loop;

a variable rate interpolator;

an NTSC interference rejection filter;

a square root Nyquist filter, coupled into the signal path in a position after the NTSC interference rejection filter; and

a second derotator coupled into the signal path in a position after the square root Nyquist filter, the second derotator adjusting the received spectrum to a baseband signal in response to the second tracking loop.

91. The digital communication system according to claim 90, further comprising a Nyquist prefilter, coupled in parallel to the signal path and in a position after the second derotator, the Nyquist prefilter and the square root Nyquist filter defining the equivalent filter.

92. The digital communication system according to claim 91, further comprising:

a real to imaginary signal converter, the converter operative to create an imaginary analogue to a real signal, the imaginary analogue having a same time stamp as the real signal; and

a time compensation circuit, coupled to time shift an imaginary component of a signal in one modulation format into an imaginary component of a signal in another modulation format.

93. The digital communication system according to claim 92, wherein the real to imaginary signal converter is a Hilbert transform filter coupled to define a Q analogue signal from an I rail signal.

94. The digital communication system according to claim 93, wherein the time compensation circuit is a Z transform circuit, having a characteristic delay $Z^{-1/2}$.

95. The digital communication system according to claim 94, wherein the characteristic delay $Z^{-1/2}$ is equal to one half a symbol time of a QAM signal.

96. (Amended) A digital communication system for receiving signals modulated in accordance with a multiplicity of modulation formats, comprising:

a front end receiving an input spectrum at an intermediate frequency;

first and second nested carrier tracking loops, the first loop acquiring carrier frequency lock in operative response to a pilot frequency component inserted into the received spectrum, the second loop providing a signal adapted to position the spectrum at a predetermined location relative to baseband in operative response to said pilot frequency component;

a third tracking loop coupled to define a symbol timing parameter in operative response to said same pilot frequency component;

an equivalent filter operating on the received spectrum in order to define a pair of symmetric signals, each of the symmetric signals centered at the characteristic frequency of the pilot frequency component when the received spectrum is at baseband; and

a decision directed carrier phase recovery loop having a phase detector operative with respect to each of the multiplicity of modulation formats.

97. The digital communication system according to claim 96, wherein the multiplicity of modulation formats includes vestigal sideband modulation (VSB), quadrature amplitude modulation (QAM) and offset-quadrature amplitude modulation (OQAM).

98. The digital communication system according to claim 97, the second tracking loop operative in conjunction with the first tracking loop to position the spectrum at a predetermined location relative to baseband when the spectrum represents a signal modulated in accordance with a first modulation format.

99. The digital communication system according to claim 98, the decision directed carrier loop operative in conjunction with the first tracking loop to position the spectrum at a predetermined location relative to baseband when the spectrum represents a signal modulated in accordance with a second modulation format.

100. The digital communication system according to claim 99, the decision directed carrier loop operative on input signals received from a maximum likelihood sequence estimation circuit integrated into an adaptive decision feedback equalizer.

101. (Amended) A digital communication system for receiving signals modulated in accordance with a multiplicity of modulation formats, comprising:

reference synthesizer circuits;

a front end receiving an input spectrum at an intermediate frequency;

first and second nested carrier tracking loops;

A12 cont'd

a symbol timing loop; and

wherein the tracking and timing loops control the reference synthesizer circuits in operative response to a passband signal centered at a frequency characteristic of an inserted pilot signal.

102. The digital communication system according to claim 101, wherein the passband signal comprises a pair of symmetric signals, each of the symmetric signals centered at the characteristic frequency of the pilot signal.

103. The digital communication system according to claim 102, wherein each of the symmetric signals includes an augmented pilot signal.

104. The digital communication system according to claim 103, wherein the passband signal is developed by an equivalent filter including a lowpass root Nyquist filter and a highpass Nyquist prefilter.